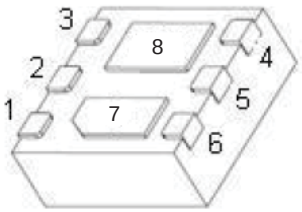
Dual P-channel MOSFET

2KJ7114DFN

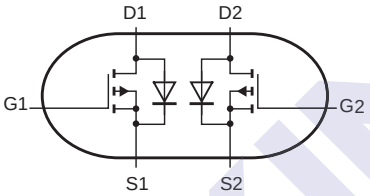
DFN2X2-6L-A



1.S1	5.G2
2.G1	6.D1
3.D2	7.D1
4.S2	8.D2

■ Features

- V_{DS} (V) = -20V
- I_D = -6.0A
- Low threshold voltage
- Very fast switching
- Trench MOSFET technology



■ Absolute Maximum Ratings (T_A = 25℃ Unless otherwise noted)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	±8	
Continuous Drain Current, t ⩽ 5 s	*1	I_D	-6.0	A
Pulsed Drain Current (tp⩽10μs)		I_{DM}	-14.4	
Power Dissipation	*1	P_D	1210	mW
	*2		515	
Thermal Resistance, Junction- to-Ambient	in free air *2	$R_{\theta JA}$	244	℃/W
	in free air *1		104	
	in free air; t ⩽ 5 s *1		64	
Junction Temperature		T_J	150	℃
Junction Storage Temperature Range		T_{stg}	-55 to 150	

*1. Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm^2.

*2. Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

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■ Electrical Characteristics (T_A = 25℃ Unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{DSS}	I_D=-10μA, V_{GS}=0V	-20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-20V, V_{GS}=0V			-1	μA
		V_{DS}=-20V, V_{GS}=0V, T_J = 150°C			-10	
Gate-Body Leakage Current	I_{GSS}	V_{DS}=0V, V_{GS}=±8V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS} , I_D=-250μA	-0.45		-0.95	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=-4.5V, I_D=-2A		28	40	mΩ
		V_{GS}=-4.5V, I_D=-2A, T_J = 150°C			65	
		V_{GS}=-2.5V, I_D=-1.5A		42	65	
		V_{GS}=-1.8V, I_D=-1A		63	100	
Forward Transconductance	g_{FS}	V_{DS}=-10V, I_D=-2A		9		S
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=-10V, f=1MHz		804		pF
Output Capacitance	C_{oss}			95		
Reverse Transfer Capacitance	C_{rss}			66		
Total Gate Charge	Q_g	V_{DS}=-10V, I_D=-2A, V_{GS} = –4.5V		6.3	9.5	nC
Gate Source Charge	Q_{gs}			1.2		
Gate Drain Charge	Q_{gd}			0.9		
Turn-On DelayTime	$t_{d(on)}$	V_{DS}=-10V, I_D=-2A, V_{GS} = –4.5 V, $R_{G(ext)}$ = 6 Ω		7		ns
Turn-On Rise Time	t_r			15		
Turn-Off DelayTime	$t_{d(off)}$			41		
Turn-Off Fall Time	t_f			14		
Maximum Body-Diode Continuous Current	I_S				-1.3	A
Diode Forward Voltage	V_{SD}	I_{SD}=-0.5 A,V_{GS}=0V			-1.2	V

■ Marking

Marking	JAQ

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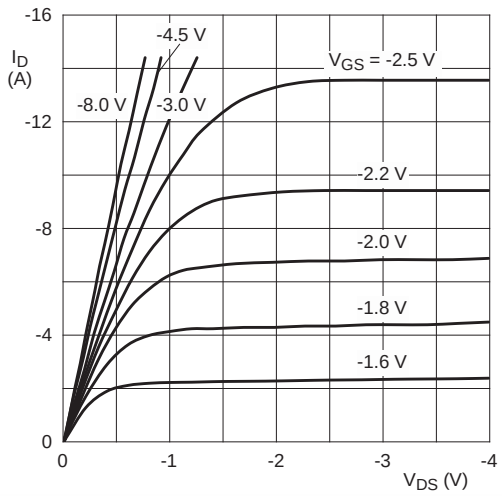
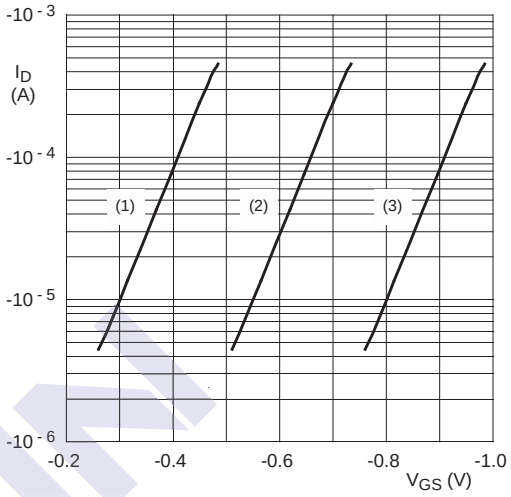
■ Typical Characterisitics



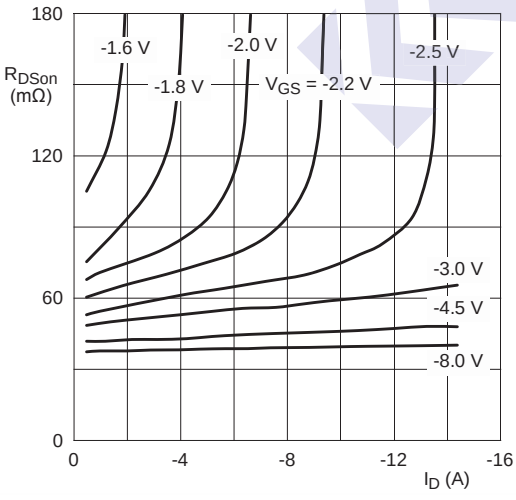
T_j = 25 °C

Fig. 1. Output characteristics: drain current as a function of drain-source voltage; typical values



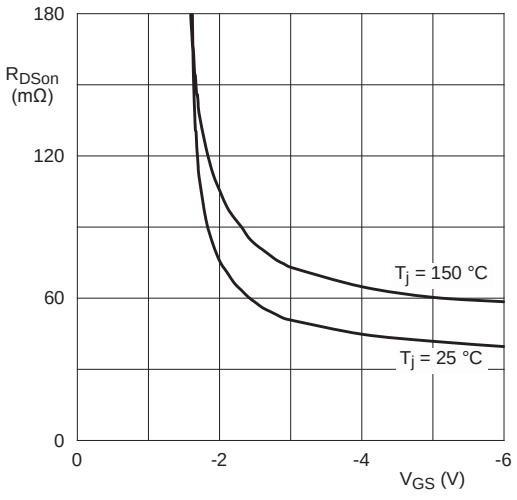
T_j = 25 °C; V_{DS} = -3 V
(1) minimum values
(2) typical values
(3) maximum values

Fig. 2. Sub-threshold drain current as a function of gate-source voltage



T_j = 25 °C

Fig. 3. Drain-source on-state resistance as a function of drain current; typical values



I_D = -2 A

Fig. 4. Drain-source on-state resistance as a function of gate-source voltage; typical values

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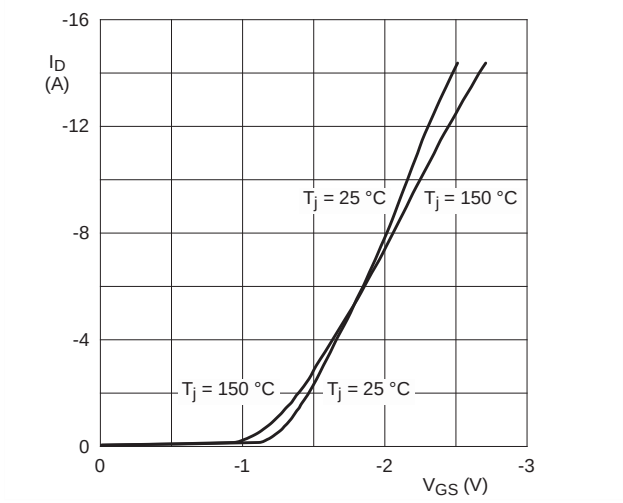


$V_{DS} > I_D \times R_{DSon}$

Fig. 5. Transfer characteristics: drain current as a function of gate-source voltage; typical values

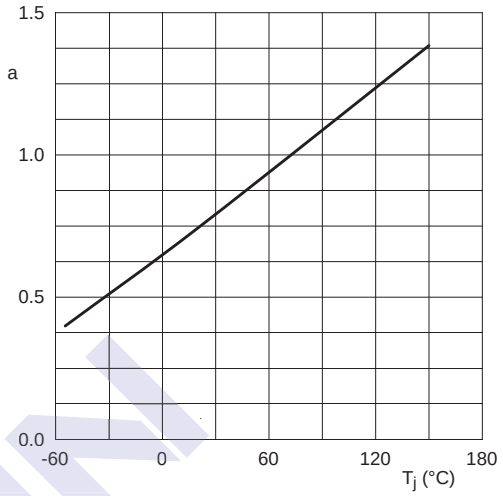
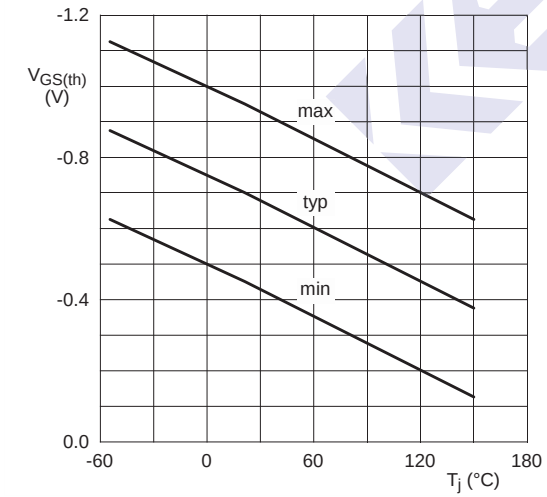


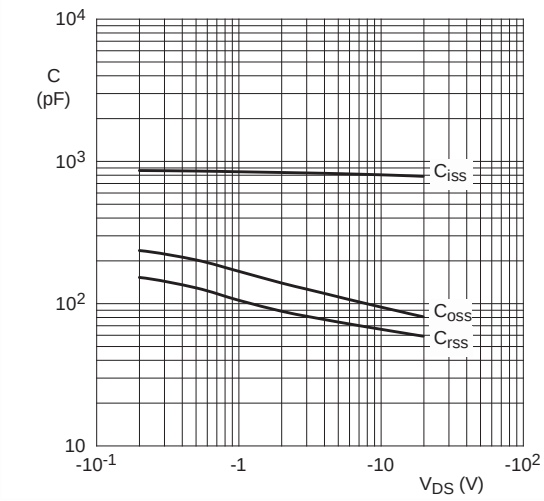
Fig. 6. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$



I_D = -0.25 mA; $V_{DS} = V_{GS}$

Fig. 7. Gate-source threshold voltage as a function of junction temperature



f = 1 MHz; V_{GS} = 0 V

Fig. 8. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

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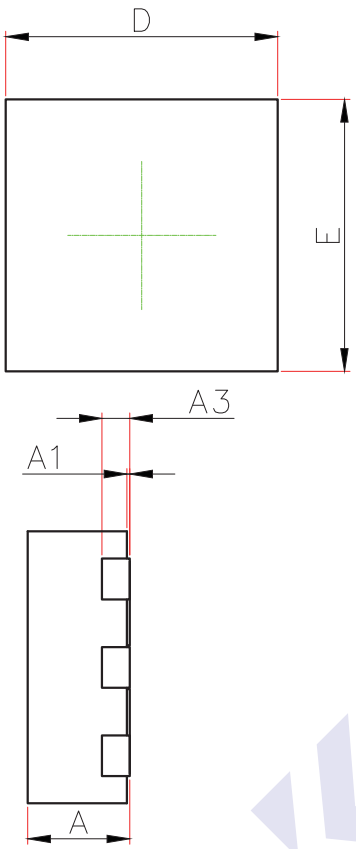
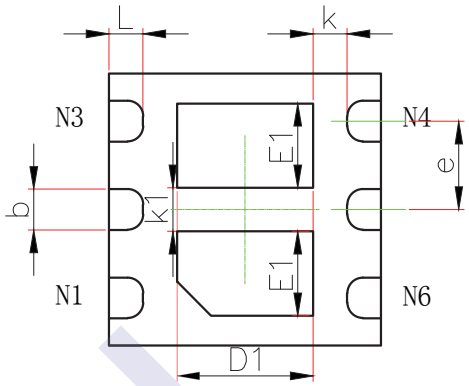
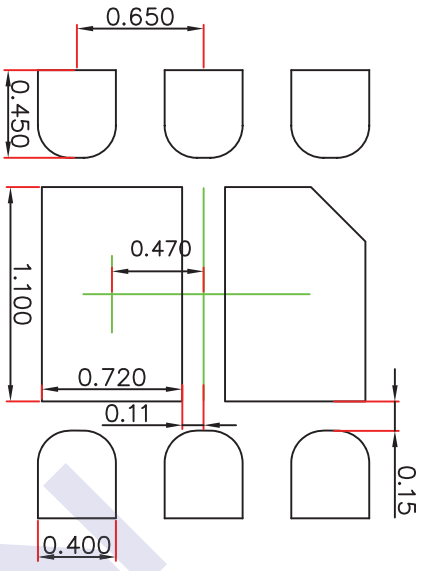
■ DFN2X2-6L-A Package Outline Dimensions





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN.	MAX.	MIN.	MAX.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	1.900	2.100	0.075	0.083
E	1.900	2.100	0.075	0.083
D1	0.900	1.100	0.035	0.043
E1	0.520	0.720	0.020	0.028
b	0.250	0.350	0.010	0.014
e	0.650TYP.		0.026TYP.	
k	0.200MIN.		0.008MIN.	
k1	0.320REF		0.013REF.	
L	0.200	0.300	0.008	0.012

■ DFN2X2-6L-A Suggested Pad Layout



Note:

1. Controlling dimension: in millimeters,
2. General tolerance: ±0.050mm,
3. The pad layout is for reference purposes only.