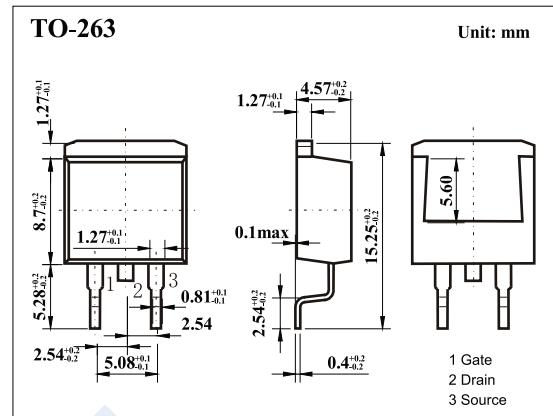
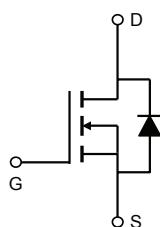


N-Channel MOSFET

2KK5093

■ Features

- $V_{DS} = 40 \text{ V}$
- $I_D (\text{at } V_{GS}=10\text{V}) = 195 \text{ A}$
- $R_{DS(\text{ON})} (\text{at } V_{GS} = 10 \text{ V}) < 1.3 \text{ m}\Omega$
- $R_{DS(\text{ON})} (\text{at } V_{GS} = 4.5 \text{ V}) < 1.8 \text{ m}\Omega$
- 100% UIS Tested
- 100% R_g Tested

■ Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	I_D	195	A
		195	
Pulsed Drain Current (Note 2)	I_{DM}	1000	
Continuous Drain Current	I_{DSM}	57	
		45.5	
Avalanche Current (Note 2)	I_{AS}	70	A
Avalanche Energy $L = 0.1\text{mH}$ (Note 2)	E_{AS}	735	mJ
Thermal Resistance, Junction- to-Ambient (Note 5)	$R_{\theta JA}$	18	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction- to-Case	$R_{\theta JC}$	0.55	
Power Dissipation (Note 4)	P_D	272	W
		136	
Power Dissipation (Note 5)	P_{DSM}	8.3	
		5.3	
Junction Temperature	T_J	175	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55 to 175	

Notes:

1. The maximum current rating is package limited.
2. Single pulse width limited by junction temperature $T_{J(\text{MAX})}=175^\circ\text{C}$.
3. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
4. The power dissipation P_D is based on $T_{J(\text{MAX})}=175^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
5. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $TA = 25^\circ\text{C}$. The Power dissipation P_{DSM} is based on $R_{\theta JA} t \leq 10\text{s}$ and the maximum allowed junction temperature of 175°C . The value in any given application depends on the user's specific board design.

N-Channel MOSFET

2KK5093

■ Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified)

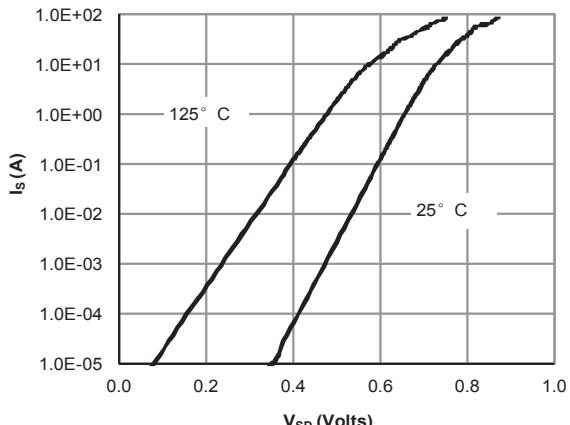
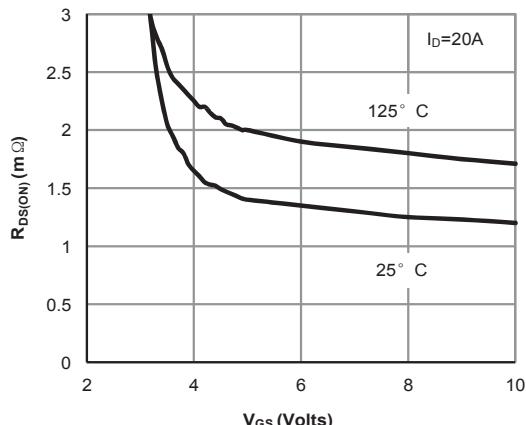
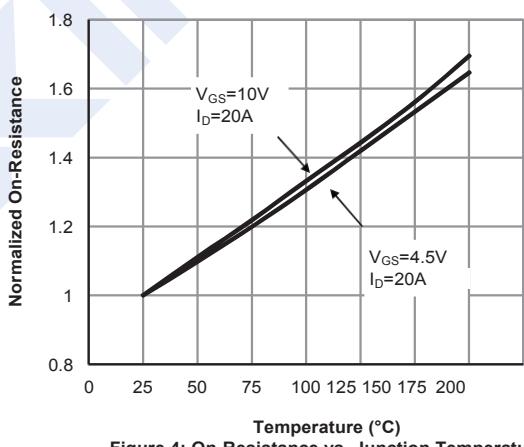
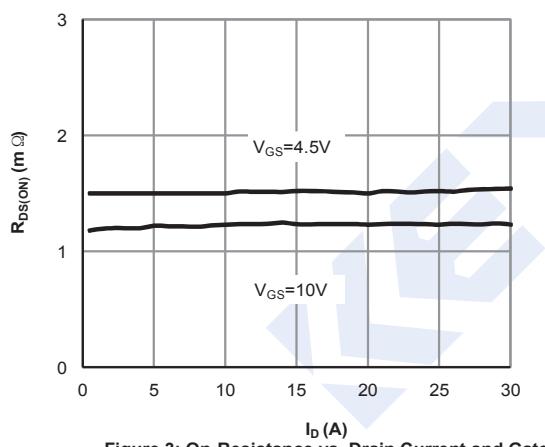
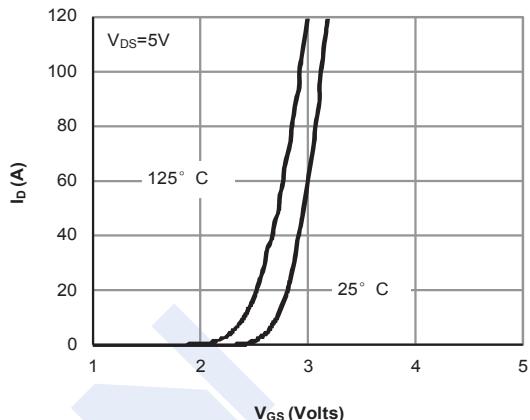
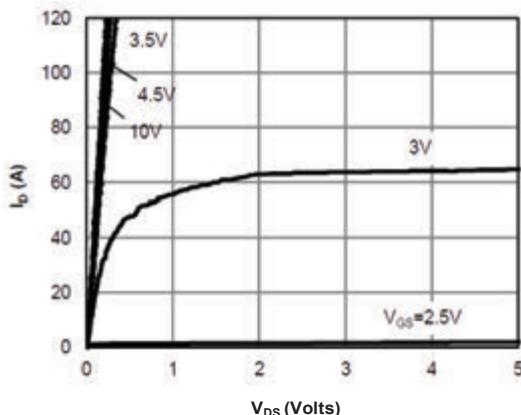
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$\text{Id} = 250 \mu\text{A}, \text{V}_{\text{GS}} = 0\text{V}$	40			V
Zero Gate Voltage Drain Current	I_{DSS}	$\text{V}_{\text{DS}} = 40 \text{ V}, \text{V}_{\text{GS}} = 0 \text{ V}$		1		μA
		$\text{V}_{\text{DS}} = 40 \text{ V}, \text{V}_{\text{GS}} = 0 \text{ V}, T_J = 55^\circ\text{C}$		5		
Gate to Source Leakage Current	I_{GSS}	$\text{V}_{\text{DS}} = 0 \text{ V}, \text{V}_{\text{GS}} = \pm 20 \text{ V}$		± 100		nA
Gate to Source Threshold Voltage	$\text{V}_{\text{GS(th)}}$	$\text{V}_{\text{DS}} = \text{V}_{\text{GS}}, \text{Id} = 250 \mu\text{A}$	1.0	2.4		V
Static Drain-Source On-Resistance	$\text{R}_{\text{DS(on)}}$	$\text{V}_{\text{GS}} = 10 \text{ V}, \text{Id} = 20 \text{ A}$		1.1	1.3	$\text{m}\Omega$
		$\text{V}_{\text{GS}} = 10 \text{ V}, \text{Id} = 20 \text{ A}, T_J = 125^\circ\text{C}$		1.6	2.0	
		$\text{V}_{\text{GS}} = 4.5 \text{ V}, \text{Id} = 20 \text{ A}$		1.4	1.8	
Forward Transconductance	g_{FS}	$\text{V}_{\text{DS}} = 5 \text{ V}, \text{Id} = 20 \text{ A}$		100		S
Dynamic Characteristics						
Input Capacitance	C_{iss}	$\text{V}_{\text{GS}} = 0 \text{ V}, \text{V}_{\text{DS}} = 20 \text{ V}, f = 1 \text{ MHz}$		9985		pF
Output Capacitance	C_{oss}			1635		
Reverse Transfer Capacitance	C_{rss}			95		
Gate Resistance	R_g	$\text{V}_{\text{GS}}=0\text{V}, \text{V}_{\text{DS}}=0\text{V}, f = 1\text{MHz}$	1.3	2.6	3.9	Ω
Switching Characteristics						
Total Gate Charge (10V)	Q_g	$\text{V}_{\text{GS}} = 10 \text{ V}, \text{V}_{\text{DS}} = 20 \text{ V}, \text{Id} = 20 \text{ A}$		128	180	nC
Total Gate Charge (4.5V)				54		
Gate Source Charge	Q_{gs}			29		
Gate Drain Charge	Q_{gd}			11		
Turn-On Delay Time	$t_{\text{d(on)}}$	$\text{V}_{\text{GS}} = 10 \text{ V}, \text{V}_{\text{DS}} = 20 \text{ V}, \text{RL} = 1 \Omega, \text{RGEN} = 3 \Omega$		16		ns
Turn-On Rise Time	t_r			16		
Turn-Off Delay Time	$t_{\text{d(off)}}$			125		
Turn-Off Fall Time	t_f			27		
Drain-Source Diode Characteristics						
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 20 \text{ A}, \frac{dI}{dt} = 500 \text{ A}/\mu\text{s}$		29		ns
Body Diode Reverse Recovery Charge	Q_{rr}			107		
Maximum Body-Diode Continuous Current	I_S	(Note 1)			195	A
Diode Forward Voltage	V_{SD}	$\text{V}_{\text{GS}} = 0 \text{ V}, I_S = 1 \text{ A}$		0.65	1	V

Notes:

6. The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.
7. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_J(\text{MAX})=175^\circ\text{C}$. The SOA curve provides a single pulse rating.
8. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$.

■ Marking

Marking	K5093 KC***
---------	----------------

N-Channel MOSFET**2KK5093****■ Typical Electrical And Thermal Characteristics**

N-Channel MOSFET

2KK5093

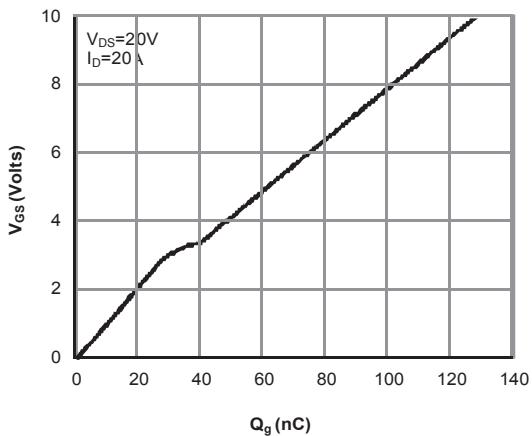


Figure 7: Gate-Charge Characteristics

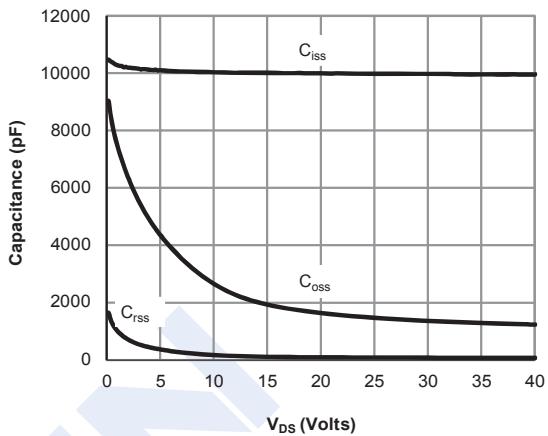


Figure 8: Capacitance Characteristics

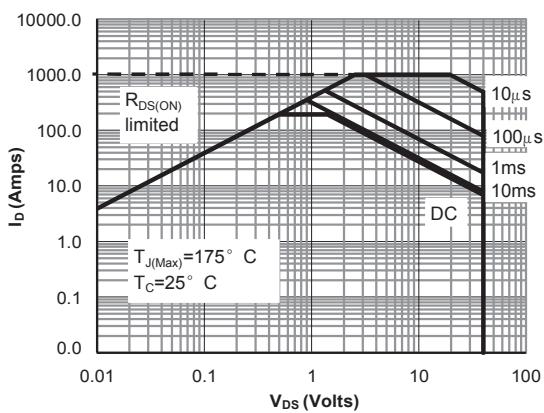


Figure 9: Maximum Forward Biased Safe Operating Area (Note 7)

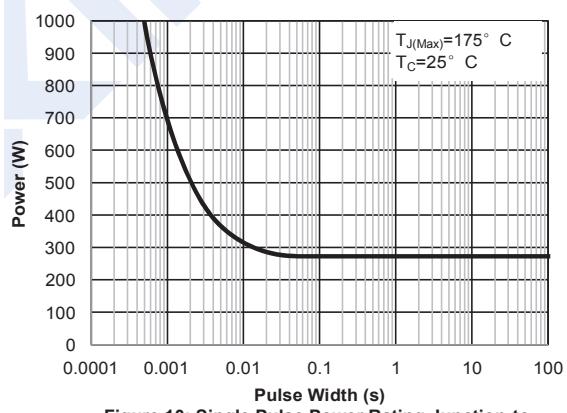


Figure 10: Single Pulse Power Rating Junction-to-Case (Note 7)

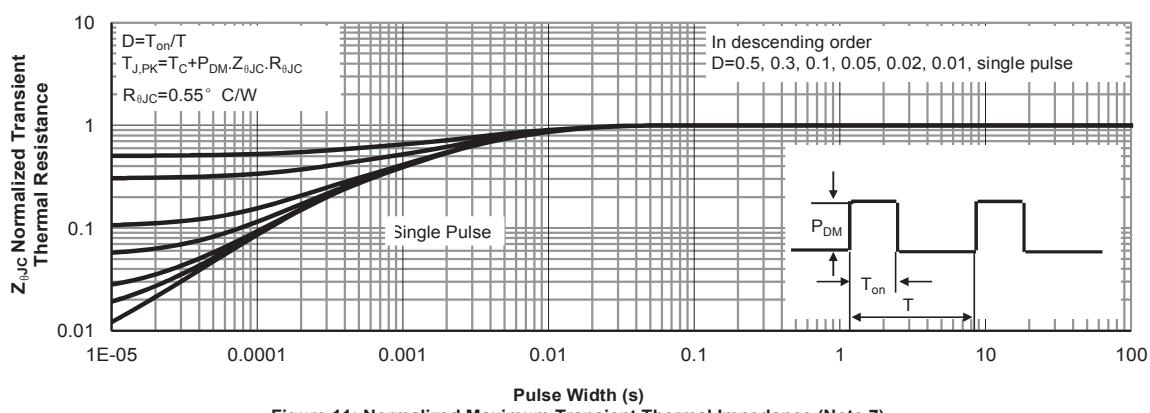


Figure 11: Normalized Maximum Transient Thermal Impedance (Note 7)

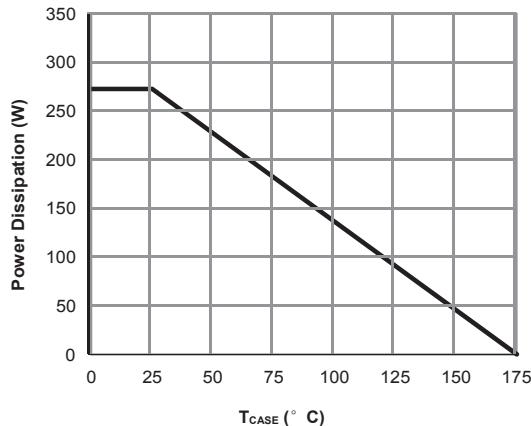
N-Channel MOSFET**2KK5093**

Figure 12: Power De-rating (Note 7)

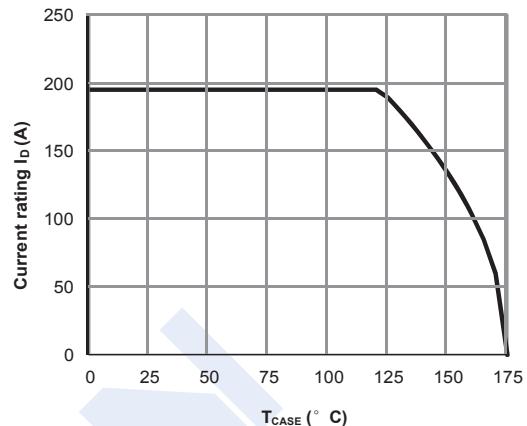


Figure 13: Current De-rating (Note 7)

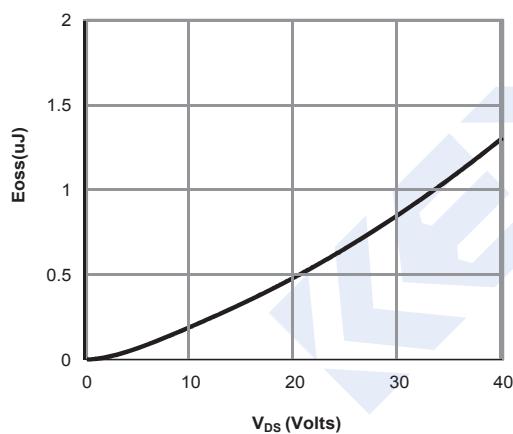


Figure 14: Coss stored Energy

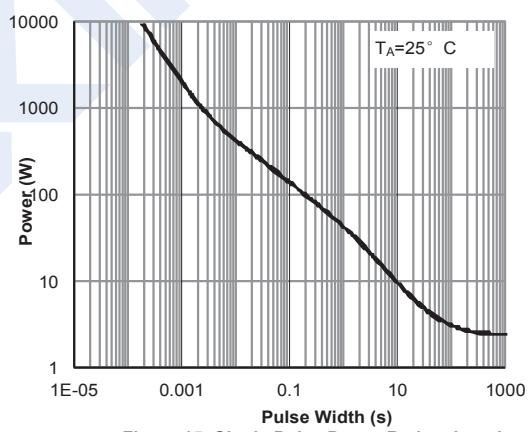


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note 8)

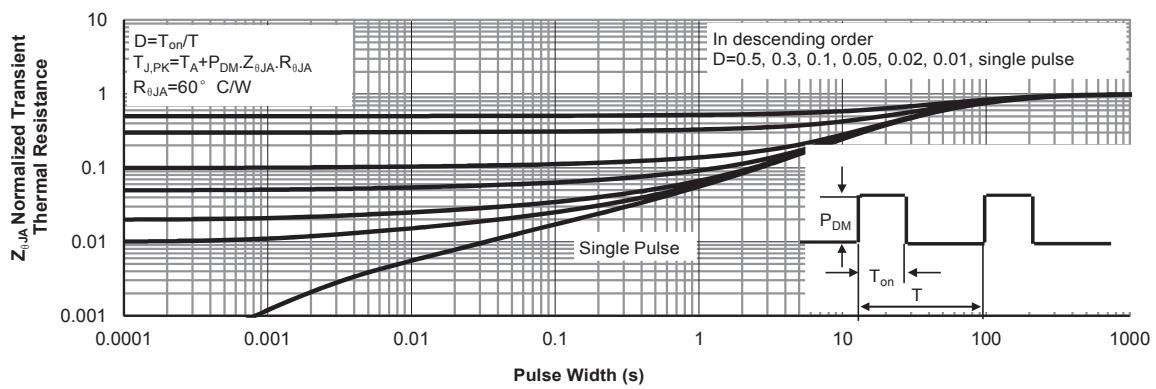
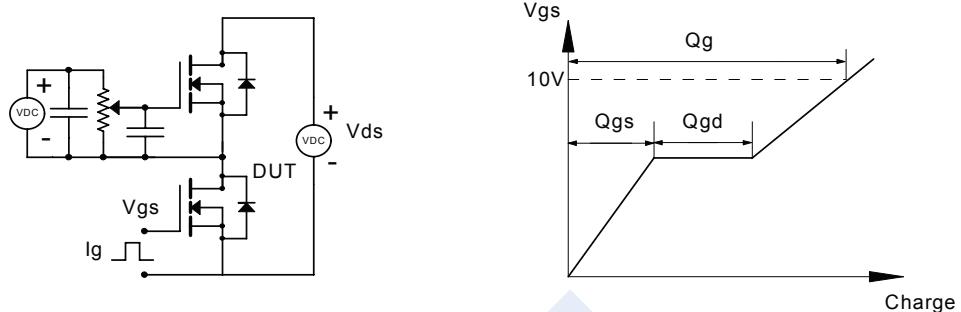


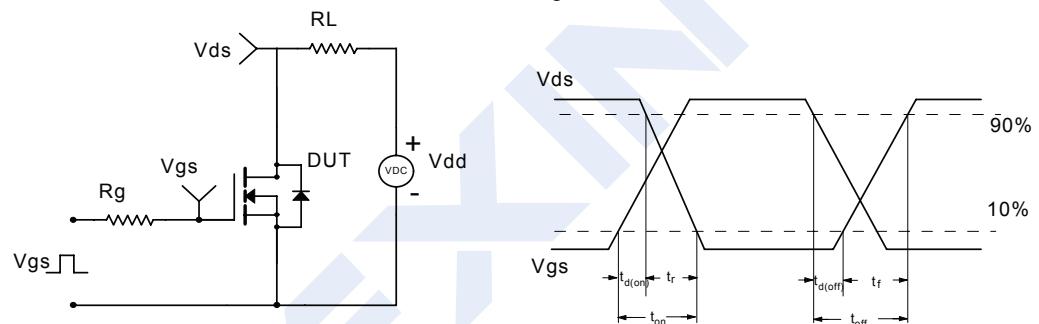
Figure 16: Normalized Maximum Transient Thermal Impedance (Note 8)

N-Channel MOSFET**2KK5093**

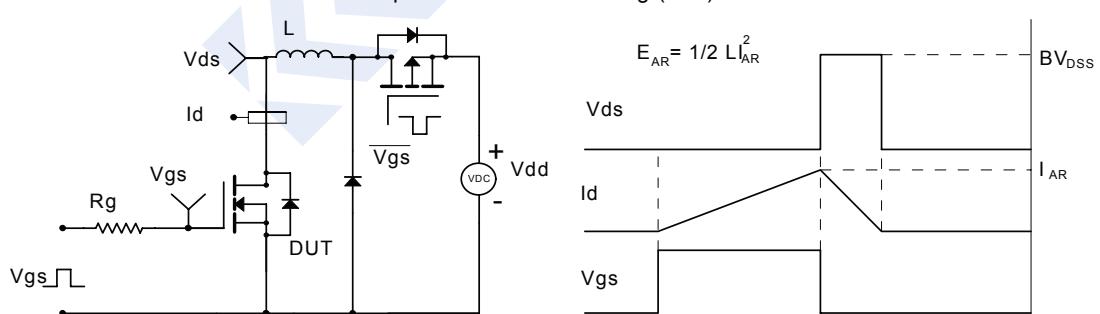
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

