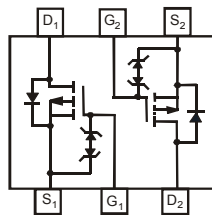


Dual P-channel MOSFET

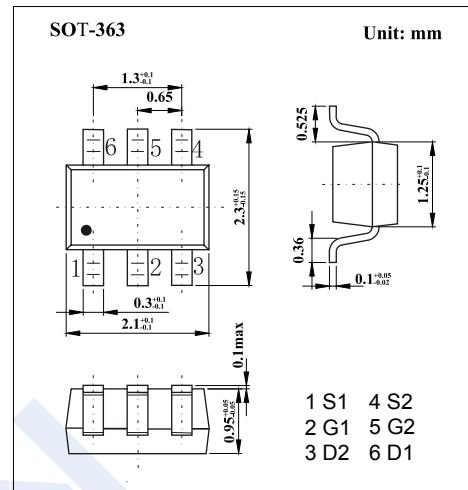
DMP2004DWK

■ Features

- V_{DS} (V) = -20V
- I_D = -540mA
- $R_{DS(on)max}$ = 0.55Ω @ $V_{GS} = 4.5V$
- Dual P-Channel MOSFET
- Low On-Resistance
- ESD Protected



Top View
Internal Schematic

■ Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless otherwise noted)

Parameter	Symbol	Rating	Unit	
Drain-Source Voltage	V_{DS}	-20	V	
Gate-Source Voltage	V_{GS}	± 8		
Continuous Drain Current	I_D	$T_A = 25^\circ\text{C}$	-430	mA
		$T_A = 85^\circ\text{C}$	-310	
Power Dissipation	P_D	250	mW	
Thermal Resistance, Junction- to-Ambient	R^{θ}_{JA}	500	$^\circ\text{C}/\text{W}$	
Junction Temperature	T_J	150	$^\circ\text{C}$	
Junction Storage Temperature Range	T_{STG}	-55 to 150		

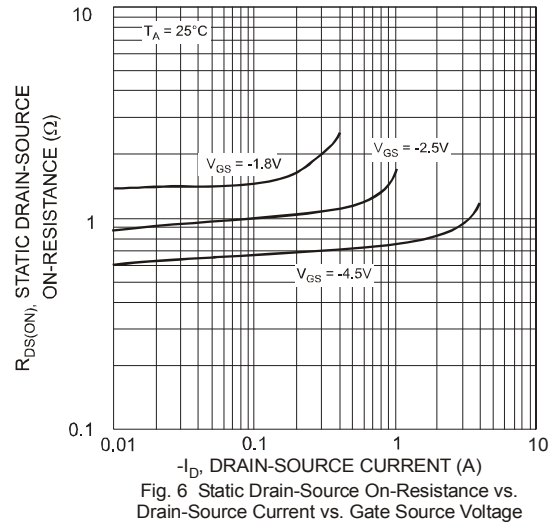
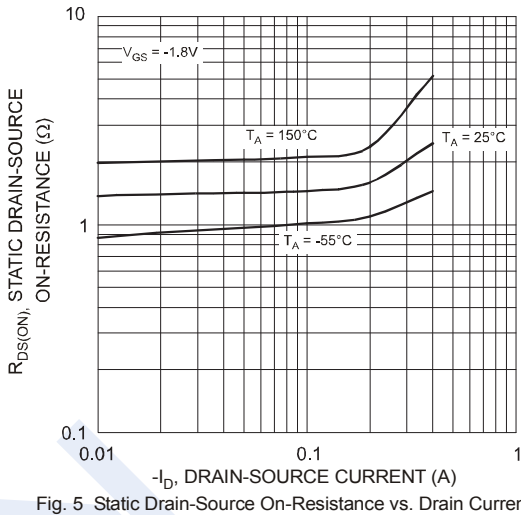
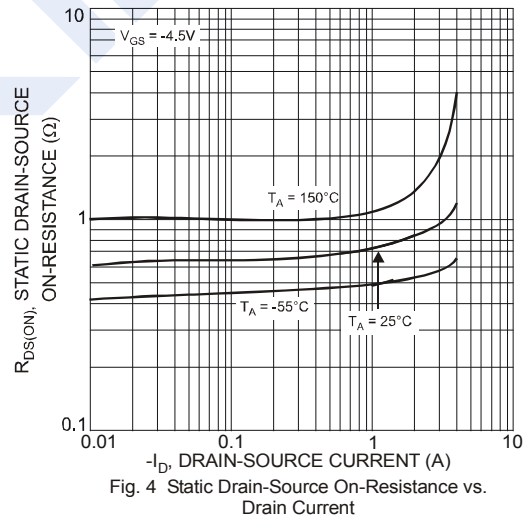
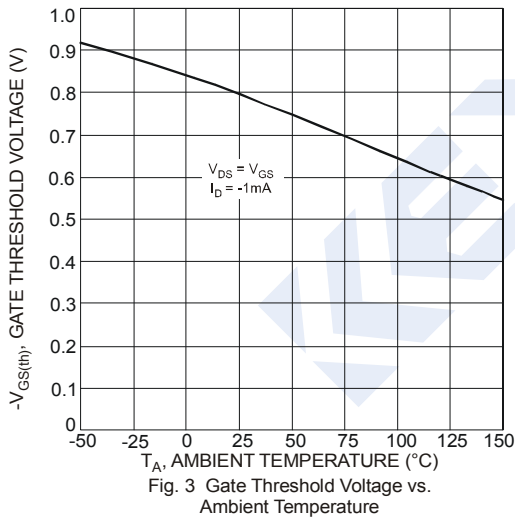
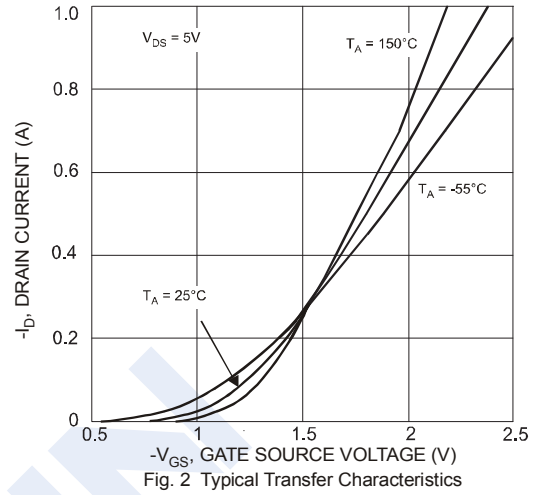
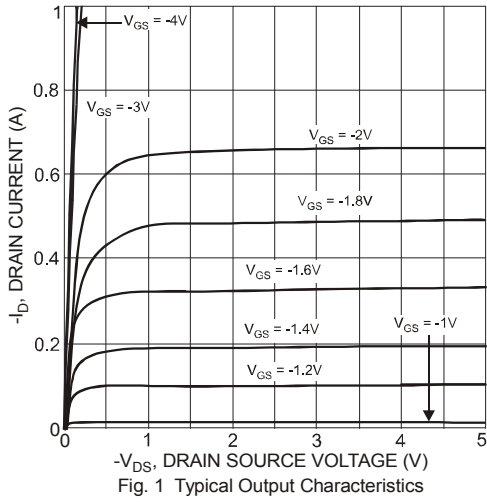
■ Electrical Characteristics ($T_A = 25^\circ\text{C}$ Unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{DSS}	$I_D = -250\mu\text{A}$, $V_{GS} = 0V$	-20			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20V$, $V_{GS} = 0V$			-1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{DS} = 0V$, $V_{GS} = \pm 4.5V$			± 1	μA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\mu\text{A}$	-0.5		-1.0	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -4.5V$, $I_D = -430\text{mA}$			0.9	Ω
		$V_{GS} = -2.5V$, $I_D = -300\text{mA}$			1.4	
		$V_{GS} = -1.8V$, $I_D = -150\text{mA}$			2.0	
Forward Transconductance	g_{FS}	$V_{DS} = -10V$, $I_D = -0.2A$	200			mS
Input Capacitance	C_{iss}	$V_{GS} = 0V$, $V_{DS} = -16V$, $f = 1\text{MHz}$			175	pF
Output Capacitance	C_{oss}				30	
Reverse Transfer Capacitance	C_{rss}				20	
Diode Forward Voltage	V_{SD}		$I_{SD} = -115\text{mA}$, $V_{GS} = 0V$			

Dual P-channel MOSFET

DMP2004DWK

■ Typical Characteristics



Dual P-channel MOSFET

DMP2004DWK

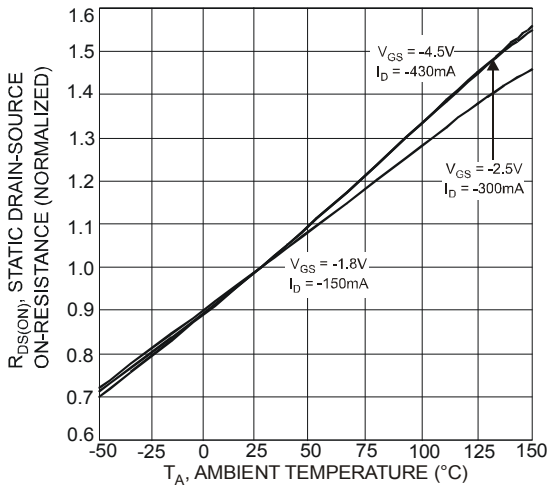


Fig. 7 Static Drain-Source On-State Resistance vs. Ambient Temperature

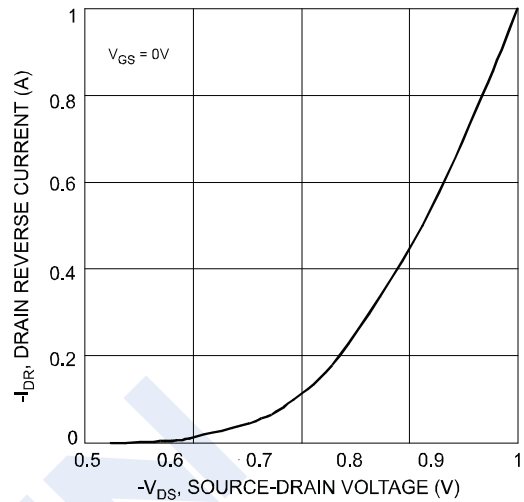


Fig. 8 Drain Reverse Current vs. Source-Drain Voltage

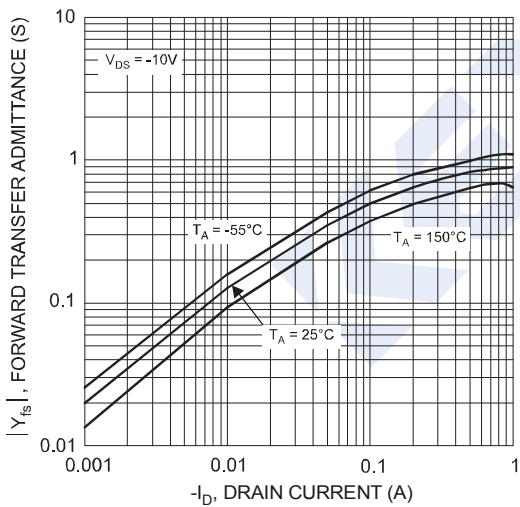


Fig. 9 Forward Transfer Admittance vs. Drain Current

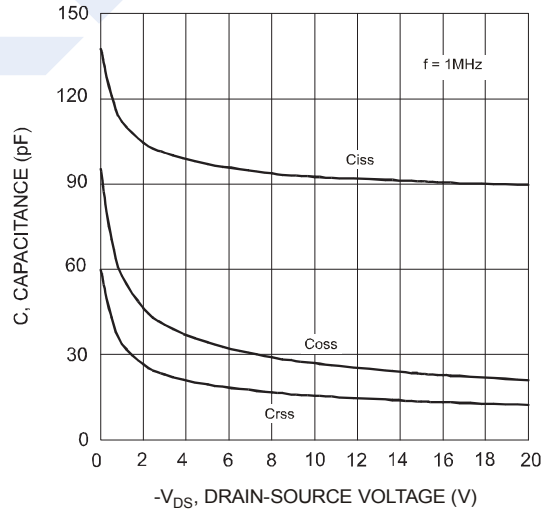


Fig. 10 Typical Capacitance